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FEE TRANSMITTAL
For FY 2007

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	10/609,634-Conf. #4954
Filing Date	July 1, 2003
First Named Inventor	Kazunari Kimino
Examiner Name	G. R. Koch
Art Unit	1734
Attorney Docket No.	R2180.0159/P159

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☐ Deposit Account Deposit Account Number: 04-1073 Deposit Account Name: Dickstein Shapiro LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fees Paid ($)**
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	**Fee ($)**	**Small Entity Fee ($)**
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	**Extra Claims**	**Fee ($)**	**Fee Paid ($)**
_____ - =	_____ x	_____ =	_____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	**Extra Claims**	**Fee ($)**	**Fee Paid ($)**
_____ - =	_____ x	_____ =	_____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims

Fee ($)	**Fee Paid ($)**
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	**Extra Sheets**	**Number of each additional 50 or fraction thereof**	**Fee ($)**	**Fee Paid ($)**
_____ - 100 =	_____ /50 =	_____ (round up to a whole number) x	_____ =	_____

4. OTHER FEE(S) **Fees Paid ($)**

Non-English Specification, $130 fee (no small entity discount)

Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal 500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent)	28,371	Telephone	(202) 420-2232
Name (Print/Type)	Thomas J. D'Amico			Date	

TRANSMITTAL OF APPEAL BRIEF

Docket No.
R2180.0159/P159

In re Application of: Kazunari Kimino

Application No.	Filing Date	Examiner	Group Art Unit
10/609,634-Conf. #4954	July 1, 2003	G. R. Koch	1734

Invention: APPARATUS AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

TO THE COMMISSIONER OF PATENTS:

Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: June 25, 2007 .

The fee for filing this Appeal Brief is $ 500.00 .

[x] Large Entity [ ] Small Entity

[ ] A petition for extension of time is also enclosed.

The fee for the extension of time is _____ .

[ ] A check in the amount of _____ is enclosed.

[ ] Charge the amount of the fee to Deposit Account No. 04-1073 .
This sheet is submitted in duplicate.

[x] Payment by credit card. Form PTO-2038 is attached.

[x] The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. 04-1073 .
This sheet is submitted in duplicate.

Dated: August 9, 2007

Thomas J. D'Amico
Attorney Reg. No. : 28,371
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2232

Docket No.: R2180.0159/P159
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Kazunari Kimino

Application No.: 10/609,634 | Confirmation No.: 4954

Filed: July 1, 2003 | Art Unit: 1734

For: APPARATUS AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE | Examiner: G. R. Koch

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on June 25, 2007, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

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This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I.	Real Party In Interest
II	Related Appeals and Interferences
III.	Status of Claims
IV.	Status of Amendments
V.	Summary of Claimed Subject Matter
VI.	Grounds of Rejection to be Reviewed on Appeal
VII.	Argument
VIII.	Conclusion
Appendix A.	Claims Appendix
Appendix B.	Evidence Appendix (none)
Appendix C.	Related Proceedings Appendix (none)

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Ricoh Company, Ltd., a corporation organized under and pursuant to the laws of Japan, and the assignee of this application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 29 claims pending in application. The application contains claims 1-11 and 23-40, which were finally rejected. This is an appeal from the final rejection of claims 1-11 and 23-40.

B. Current Status of Claims

1. Claims canceled: 12-22.

2. Claims withdrawn from consideration but not canceled: None.

3. Claims pending: 1-11 and 23-40.

4. Claims allowed: None.

5. Claims rejected: 1-11 and 23-40.

C. Claims On Appeal

The claims on appeal are claims 1-11 and 23-40.

IV. STATUS OF AMENDMENTS

There has been no amendment subsequent to the February 23, 2007 Final Rejection. A Request for Reconsideration was filed May 23, 2007. An Advisory Action was issued by the Examiner, dated June 4, 2007.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention is directed to "an apparatus and a method for manufacturing semiconductor devices, and more particularly, to such apparatus and method implemented with improved steps of forming a sealant resin layer on the surface of a wafer substrate provided thereon with electrodes." Specification, paragraph [0001].

"In the resin sealing process for fabricating the chip-size package, sealant resin layers can be formed by spin-coating raw resin layer or by heat molding under pressurization in a metal mold, for example. In the spin-coating method for forming the sealant resin layer, however, a drawback is that additional steps must be taken for forming a coating layer at the tip of the protruded electrode, as noted earlier, thereby complicating the process. In addition, other drawbacks are encountered in the method of spin coating such as wasteful use of resinous material and difficulty in precise control of raw sealant resin layer especially in the vicinity of protruded electrodes." Paragraph [0006].

"In the method using metal molds, disadvantages are that various kinds of molds have to be provided corresponding to each wafer substrate with different specification, and that polishing steps are required for exposing tip portions of electrodes, to thereby increase manufacturing costs." Paragraph [0007] (emphasis added).

There is "a difficulty in handling the thus prepared sealant resin layer, in which chipping off of the resin layer may arise during dicing steps or conveying steps following the carving out of the semiconductor devices." Paragraph [0008].

Accordingly, independent claim 1 recites an apparatus for manufacturing a semiconductor device (FIG. 2, paragraph [0051]), comprising: a substrate holding unit (3)

for holding a semiconductor wafer substrate (1), wherein said semiconductor wafer substrate (1) is provided with at least one electrode (43/41) formed on a first surface (1a) thereof (FIGs. 1A and 2, paragraphs [0051] and [0064]); a discharging mechanism (11) for discharging droplets (29) of raw sealant resin contained in a resin container unit (15) through at least one discharging nozzle (13) onto said first surface (1a) of said semiconductor wafer substrate (1) held on said substrate holding unit (3) (FIG. 3B, paragraphs [0057]-[0058]); and a drive mechanism (9) for displacing at least one of said semiconductor wafer substrate (1) and said discharging nozzle (13) (FIG. 2, paragraph [0054]).

Claim 1 further recites a control unit (33) for controlling said discharging mechanism (11) and said drive mechanism (9) such that said raw sealant resin is attached to said first surface (1a) of said semiconductor wafer substrate (1) excluding at least a portion of said electrode (FIG. 2, paragraphs [0061] and [0071]); and an image information device (31) for capturing image information of said semiconductor wafer substrate (1) prior to said raw sealant resin being discharged from said discharging mechanism (11); said image information device (31) configured to provide said image information to said control unit (33) (FIG. 2, paragraphs [0055] and [0070]-[0071]), wherein said control unit (33) is constructed to calculate a position based on said image information for said drive mechanism (9) to displace said at least one of said semiconductor wafer substrate (1) and said discharging nozzle (13), and for said discharging mechanism (11) to discharge said droplets (29) of raw sealant resin on said first surface (1a) of said semiconductor wafer substrate (1) excluding said at least a portion of said electrode (43) (FIG. 2, paragraphs [0055] and [0070]-[0071]).

Independent claim 23 recites an apparatus for manufacturing a semiconductor device (FIG. 2, paragraph [0051]), comprising: substrate holding means (3) for holding a semiconductor wafer substrate (1), wherein said substrate (1) is provided with at least one electrode (43/41) formed on a first surface (1a) thereof (FIGs. 1A and 2, paragraphs [0051] and [0064]); means for discharging (11) droplets (29) of raw sealant resin contained in a resin container unit (15) through at least one discharging nozzle (13) onto said first surface (1a) of said semiconductor wafer substrate (1) held on said substrate holding unit (3) (FIG. 3B, paragraphs [0057]-[0058]); and drive means (9) for displacing at least one of said semiconductor wafer substrate (1) and said discharging nozzle (13) (FIG. 2, paragraph [0054]).

Claim 23 further recites means for controlling (33) a discharging mechanism (11) and a drive mechanism (9) such that said raw sealant resin is attached to said first surface (1a) of said semiconductor wafer substrate (1) excluding at least a portion of said electrode (43) (FIG. 2, paragraphs [0061] and [0071]); means for capturing image information (31) of said semiconductor wafer substrate (1) prior to droplets (29) of raw sealant resin being discharged by said discharging means (11) (FIG. 2, paragraphs [0055] and [0070]-[0071]); means for providing image information of said semiconductor wafer substrate (1) (FIG. 2, paragraph [0055], dashed line connecting 31 to 33); and means for calculating a position (33), based upon said image information, for said discharging mechanism (11) to discharge said droplets (29) of raw sealant resin on said first surface (1a) of said semiconductor wafer substrate (1) excluding at least a portion of said electrode, and for said drive mechanism (9) to displace at least one of said semiconductor wafer substrate (1) and said discharging nozzle (13) (FIG. 2, paragraphs [0055] and [0070]-[0071]).

Independent claim 34 recites a semiconductor device manufacturing apparatus (FIG. 2, paragraph [0051]), comprising: a semiconductor wafer substrate (1), said semiconductor wafer substrate (1) having at least one electrode (43/41) on a first surface (1a) thereof, and wherein said semiconductor wafer substrate (1) is held in a substrate holding unit (3) (FIGs. 1A and 2, paragraphs [0051] and [0064]); at least one discharging head (11) for discharging droplets (29) of raw sealant resin on said semiconductor wafer substrate (1) and having at least one discharging nozzle (13) (FIG. 3B, paragraphs [0057]-[0058]); a resin container unit (15) connected to said discharging head (11) and containing raw sealant resin (FIG. 3B, paragraphs [0057]-[0058]); and a drive mechanism (9) for displacing at least one of said semiconductor wafer substrate (1) and said discharging head (11) (FIG. 2, paragraph [0054]).

Claim 34 further recites an image information camera (31) for capturing image information of said semiconductor wafer substrate (1) prior to said raw sealant resin being discharged by said discharging head (13); said image information device (31) configured to provide said image information of said semiconductor wafer substrate (1) (FIG. 2, paragraphs [0055] and [0070]-[0071]); and a control unit (33) for controlling said discharging head (11) and said drive mechanism (9) (FIG. 2, paragraphs [0061] and [0071]), wherein said control unit (33) is adapted to calculate a position, based on said image information, for said discharging head (11) to discharge droplets (29) of raw sealant resin on said semiconductor wafer substrate (1) excluding said at least one electrode (43), and for said drive mechanism (9) to displace said at least one of said semiconductor wafer substrate (1).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether claims 1-2, 6-8, 10-11, 23-24, 28-30, and 32-33 are properly rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,711,989 to Ciardella (hereinafter "Ciardella I").

B. Whether claims 1-2, 4, 6-8, 10-11, 23-24, 26, 28-30, 32-36, 38, and 40 are properly rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,906,682 to Bouras (hereinafter "Bouras") with reference to U.S. Patent No. 5,505,777 to Ciardella (hereinafter "Ciardella II") (incorporated by reference into Bouras).

C. Whether claims 4, 26, 34-36, 38, and 40 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Ciardella I in view of Bouras.

D. Whether claims 3, 5, 25, 27, 31, and 37 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Ciardella I, or Bouras/Ciardella II, or Ciardella I in view of Bouras, in view of U.S. Patent No. 5,935,375 to Nakazawa et al. (hereinafter "Nakazawa").

E. Whether claims 5, 9, 27, 31, and 39 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Ciardella I, or Bouras/Ciardella II, or Ciardella I in view of Bouras, in view of U.S. Patent No. 6,007,631 to Prentice (hereinafter "Prentice").

F. Whether claims 5, 9, 27, 31, and 39 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Ciardella I, or Bouras/Ciardella II, or

Ciardella I in view of Bouras, in view of U.S. Patent No. 6,017,392 to Cavallaro (hereinafter "Cavallaro").

VII. ARGUMENT

A. Claims 1-2, 6-8, 10-11, 23-24, 28-30, and 32-33 are Not Anticipated by the Disclosure of Ciardella I.

Claim 1 recites an apparatus for manufacturing a semiconductor device comprising, *inter alia*, "an image information device for capturing image information of said semiconductor wafer substrate prior to said raw sealant resin being discharged from said discharging mechanism; said image information device configured to provide said image information to said control unit, wherein said control unit is constructed to calculate a position based on said image information for said drive mechanism to displace said at least one of said semiconductor wafer substrate and said discharging nozzle, and for said discharging mechanism to discharge said droplets of raw sealant resin on said first surface of said semiconductor wafer substrate" (emphasis added). Claim 23 recites means for performing similar functions. Appellant respectfully submits that Ciardella I does not disclose these limitations.

It should be noted that in a telephonic conversation with the Examiner on May 15, 2007, Appellant's representative confirmed that the rejection was made with reference to Ciardella I FIG. 2 (with related reference numbers), and not to FIG. 5 (as in later rejections with reference to Bouras).

To the contrary, Ciardella I discloses that the "video camera of the assembly 16 includes a charge coupled device (CCD) whose output is converted to digital form and processed in determining ... the location ... of a selected dot dispensed onto the circuit

board 36." Col. 4, ln. 34-39. Therefore, Ciardella I discloses only using the video for determining the location of a dot already dispensed. Appellant respectfully submits that Ciardella I does not disclose, teach, or suggest an image information device for capturing image information prior to said raw sealant resin being discharged from said discharging mechanism, as recited in claims 1 and 23. Since Ciardella I does not disclose all of the limitations of claims 1 and 23, claims 1 and 23 are not anticipated by Ciardella I.

Claims 2, 6-8, 10-11, 24, 28-30, and 32-33 depend, respectively, from independent claims 1 and 23, and are patentable at least for the reasons mentioned above, and on their own merits.

For example, claims 2 and 24 recite that the "electrode formed on said first surface of said semiconductor wafer substrate is a protruded-shaped electrode" and that the "control unit is adapted to control said discharging mechanism and said drive mechanism such that said raw sealant resin is attached to said first surface except a tip portion of said protruded-shaped electrode." The February 23, 2007 Final Office Action did not provide any support for the rejection. In fact, Ciardella I does not disclose these limitations. Rather, Ciardella I discloses only that drops of adhesive are deposited on the circuit board. Col. 3, ln. 43-45. Ciardella is silent with respect to an electrode, a protruded-shaped electrode, tip portions of a protruded-shaped electrode, or "raw sealant resin [being] attached to said first surface except a tip portion of said protruded-shaped electrode," as recited in claims 2 and 24.

Moreover, claims 7 and 29 recite that the "control unit controls said discharging mechanism and said drive mechanism such that said raw sealant resin is not attached to at least a portion of dicing lines of said semiconductor wafer substrate." Claims 8, 11, 30, and

33 also recite "that said raw sealant resin is not attached to dicing lines of said semiconductor wafer substrate." Claims 10 and 32 recite "that said raw sealant resin is not attached to at least a portion of dicing lines of said semiconductor wafer substrate." The February 23, 2007 Final Office Action did not provide any support for these rejections. In fact, Ciardella I does not disclose these limitations. Rather, Ciardella I discloses only that drops of adhesive are deposited on the circuit board. Col. 3, ln. 43-45. Ciardella I is silent with respect to dicing lines, and therefore does not disclose, teach, or suggest that raw sealant resin is not attached to at least a portion of dicing lines of said semiconductor wafer substrate as recited in claims 7, 10, 29, and 32. Ciardella I also does not disclose, teach, or suggest that raw sealant resin is not attached to dicing lines of said semiconductor wafer substrate as recited in claims 8, 11, 30, and 33.

Appellant respectfully requests that the 35 U.S.C. § 102(b) rejection of claims 1-2, 6-8, 10-11, 23-24, 28-30, and 32-33 be reversed.

B. Claims 1-2, 6-8, 10-11, 23-24, 28-30, and 32-33 are Not Anticipated by the Disclosure of Bouras, Even with Reference to Ciardella II.

Claim 1 recites an apparatus for manufacturing a semiconductor device comprising, *inter alia*, "an image information device for capturing image information of said semiconductor wafer substrate prior to said raw sealant resin being discharged from said discharging mechanism; said image information device configured to provide said image information to said control unit, wherein said control unit is constructed to calculate a position based on said image information for said drive mechanism to displace said at least one of said semiconductor wafer substrate and said discharging nozzle, and for said discharging mechanism to discharge said droplets of raw sealant resin on said first surface of said semiconductor wafer substrate excluding said at least a portion of said electrode"

(emphasis added). Claims 23 and 34 recite similar limitations. Appellant respectfully submits that Bouras, even with reference to Ciardella II, does not disclose these limitations.

To the contrary, Bouras discloses that the "desired quantity of adhesive is sufficient to ensure that each of the solder ball-to-solder pad connections of the flip chip 10 is encapsulated with liquid epoxy." Col. 6, ln. 32-36. Appellant respectfully submits that Bouras does not disclose, teach, or suggest a control unit configured to control said discharging mechanism to discharge said droplets excluding said at least a portion of said electrode, as recited in claims 1, 23, and 34. Nor is Ciardella II cited for these limitations. Thus, Ciardella II does not remedy the deficiencies of Bouras. Since Bouras, even with reference to Ciardella II, does not disclose all of the limitations of claims 1, 23, and 34, claims 1, 23, and 34 are not anticipated by Bouras.

Claims 2, 4, 6-8, 10-11, 24, 26, 28-30, 32-33, 35-36, 38, and 40 depend, respectively, from independent claims 1, 23, and 34, and are patentable at least for the reasons mentioned above, and on their own merits.

For example, claims 2, 24, and 36 recite that the "control unit is adapted to control said discharging mechanism and said drive mechanism such that said raw sealant resin is attached to said first surface except a tip portion of said protruded-shaped electrode." As discussed above, Bouras discloses that the "desired quantity of adhesive is sufficient to ensure that each of the solder ball-to-solder pad connections of the flip chip 10 is encapsulated with liquid epoxy." Col. 6, ln. 32-36. Appellant respectfully submits that Bouras does not disclose, teach, or suggest that raw sealant resin is attached to said first surface except a tip portion of said protruded-shaped electrode, as recited in claims 2, 24, and 36.

Moreover, claims 7 and 29 recite that the "control unit controls said discharging mechanism and said drive mechanism such that said raw sealant resin is not attached to at least a portion of dicing lines of said semiconductor wafer substrate." Claims 8, 11, 30, and 33 also recite "that said raw sealant resin is not attached to dicing lines of said semiconductor wafer substrate." Claims 10 and 32 recite "that said raw sealant resin is not attached to at least a portion of dicing lines of said semiconductor wafer substrate." The February 23, 2007 Final Office Action did not provide any support for these rejections. In fact, Bouras does not disclose these limitations. Rather, Bouras discloses that drops of adhesive are deposited on the circuit board (Col. 3, ln. 43-45) and the "semiconductor die or flip chip 10 (FIG. 1) is provided with a pattern of solder bumps or balls 12 on an underside or circuit side thereof" (Col. 1, ln. 41-43). Bouras is silent with respect to dicing lines, and therefore does not disclose, teach, or suggest that raw sealant resin is not attached to at least a portion of dicing lines of said semiconductor wafer substrate as recited in claims 7, 10, 29, and 32. Bouras also does not disclose, teach, or suggest that raw sealant resin is not attached to dicing lines of said semiconductor wafer substrate as recited in claims 8, 11, 30, and 33.

Appellant respectfully requests that the 35 U.S.C. § 102(b) rejection of claims 1-2, 4, 6-8, 10-11, 23-24, 26, 28-30, 32-36, 38, and 40 be reversed.

C. Claims 4, 26, 34-36, 38, and 40 would not have been obvious under 35 U.S.C. § 103(a) from the combined disclosures of Ciardella I and Bouras.

Claims 4 and 26 depend, respectively, from claims 1 and 23, and are patentable at least for the reasons mentioned above, and on their own merits.

In order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. §2142. Neither Ciardella I nor Bouras, even when considered in combination, teaches or suggests all limitations of independent claim 34. As described above, Bouras does not teach all of the limitations of claim 34. Furthermore, claim 34 recites limitations similar to claims 1 and 23; therefore, Bouras does not cure the above-discussed deficiencies of Ciardella I. Therefore, claim 34 and dependent claims 35-36, 38, and 40 are not obvious over the cited combination.

In addition, claim 36 recites that the "control unit is adapted to control said discharging mechanism and said drive mechanism such that said raw sealant resin is attached to said first surface except a tip portion of said protruded-shaped electrode." As discussed above, Bouras discloses that the "desired quantity of adhesive is sufficient to ensure that each of the solder ball-to-solder pad connections of the flip chip 10 is encapsulated with liquid epoxy." Col. 6, ln. 32-36. Appellant respectfully submits that Bouras does not disclose, teach, or suggest that raw sealant resin is attached to said first surface except a tip portion of said protruded-shaped electrode, as recited in claim 36.

Appellant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 4, 26, 34-36, 38, and 40 be reversed.

D. Claims 3, 5, 25, 27, 31, and 37 would not have been obvious under 35 U.S.C. § 103(a) from the combined disclosures of Ciardella I and Nakazawa; Bouras/Ciardella II and Nakazawa; or Ciardella I, Bouras, and Nakazawa.

Claims 3, 5, 25, 27, 31, and 37 depend, respectively, from claims 1, 23, and 34, and are patentable at least for the reasons mentioned above, and because Nakazawa, which has been cited as teaching "a plurality of discharging nozzles" fails to cure the deficiencies of Ciardella I, Bouras/Ciardella II, and the Ciardella I and Bouras combination. Appellant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 3, 5, 25, 27, 31, and 37 be reversed.

E. Claims 5, 9, 27, 31, and 39 would not have been obvious under 35 U.S.C. § 103(a) from the combined disclosures of Ciardella I and Prentice; Bouras/Ciardella II and Prentice; or Ciardella I, Bouras, and Prentice.

Claims 5, 9, 27, 31, and 39 depend, respectively, from claims 1, 23, and 34, and are patentable at least for the reasons mentioned above, and because Prentice, which has been cited as teaching "two kinds of discharging mechanisms" fails to cure the deficiencies of Ciardella I, Bouras/Ciardella II, and the Ciardella I and Bouras combination. Appellant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 5, 9, 27, 31, and 39 be reversed.

F. Claims 5, 9, 27, 31, and 39 would not have been obvious under 35 U.S.C. § 103(a) from the combined disclosures of Ciardella I and Cavallaro; Bouras/Ciardella II and Cavallaro; or Ciardella I, Bouras, and Cavallaro.

Claims 5, 9, 27, 31, and 39 depend, respectively, from claims 1, 23, and 34, and are patentable at least for the reasons mentioned above, and because Cavallaro, which has been cited as teaching "two kinds of discharging mechanisms" fails to cure the deficiencies of Ciardella I, Bouras/Ciardella II, and the Ciardella I and Bouras combination. Appellant

respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 5, 9, 27, 31, and 39 be reversed.

In addition, in the "Response to Arguments" section, the February 23, 2007 Final Office Action asserts that "in response to Appellant's argument that the imaging functions are different, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art." Final Office Action, page 2. The Office Action also adds that if the "prior art structure is capable of performing the intended use, then it meets the claim." Final Office Action, page 2. Appellant respectfully submits that the claims are not directed toward an "intended use," but toward an apparatus configured to perform specific actions.

Specifically, the claimed apparatus, as embodied by independent claims 1, 23, and 34, includes an image information device for capturing image information of a semiconductor wafer substrate before droplets of raw sealant is discharged onto the substrate. Furthermore, the image information device is configured to provide the image information to a control unit. The control unit is constructed to calculate a position for discharging droplets of raw sealant resin on a first surface of the substrate based upon the image information. As such, the limitations of claims 1, 23, and 34 define a structure which is different from that disclosed in the cited references.

Moreover, as a matter of law, "statements of intended use ... may ... limit apparatus claims ... if the Appellant clearly and unmistakably relied on those uses ... to distinguish prior art." *Catalina Marketing Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 809, 62 U.S.P.Q.2d 1781 (Fed. Cir. 2002). Furthermore, a limitation including an element "for"

performing a function is a structural limitation. *See In re Shaffer*, 108 USPQ 326, 329 (CCPA 1956) (circuit for attenuating is a structure). This is the case here, because Appellant is relying on all of the claim limitations, including those deemed "intended use" by the Office Action, to distinguish over the prior art which fails to teach or suggest claim limitations.

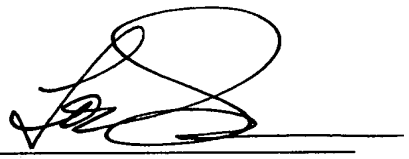
In addition, the "means for" limitations of claims 23-33 do not fall under MPEP § 2114, as indicated by the Office Action. Rather, the "means for" limitations are "means plus function" limitations in accordance with MPEP § 2181. According to the MPEP, "where means plus function language is used to define the characteristics of a machine..., such language must be interpreted to read on only the structure ... disclosed in the specification and 'equivalents thereof' that correspond to the recited function." MPEP § 2106(II)(C). Again, these are structure claims and the limitations simply cannot be ignored.

VIII. CONCLUSION

For each of the foregoing reasons, Appellant respectfully submits that the claimed invention is novel and non-obvious over the cited prior art. Reversal of each of the final grounds of rejection is respectfully solicited.

Dated: August 9, 2007

Respectfully submitted,



By_____

Thomas J. D'Amico
Registration No.: 28,371
Rachael Lea Leventhal
Registration No.: 54,266
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Appellant

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/609,634

1. (Previously Presented) An apparatus for manufacturing a semiconductor device, comprising:

a substrate holding unit for holding a semiconductor wafer substrate, wherein said semiconductor wafer substrate is provided with at least one electrode formed on a first surface thereof;

a discharging mechanism for discharging droplets of raw sealant resin contained in a resin container unit through at least one discharging nozzle onto said first surface of said semiconductor wafer substrate held on said substrate holding unit;

a drive mechanism for displacing at least one of said semiconductor wafer substrate and said discharging nozzle;

a control unit for controlling said discharging mechanism and said drive mechanism such that said raw sealant resin is attached to said first surface of said semiconductor wafer substrate excluding at least a portion of said electrode; and

an image information device for capturing image information of said semiconductor wafer substrate prior to said raw sealant resin being discharged from said discharging mechanism; said image information device configured to provide said image information to said control unit,

wherein said control unit is constructed to calculate a position based on said image information for said drive mechanism to displace said at least one of said semiconductor wafer substrate and said discharging nozzle, and for said discharging mechanism to discharge said droplets of raw sealant resin on said first surface of said semiconductor wafer substrate excluding said at least a portion of said electrode.

2. (Original) The apparatus for manufacturing a semiconductor device according to claim 1, wherein said electrode formed on said first surface of said semiconductor wafer substrate is a protruded-shaped electrode, and wherein said control unit is adapted to control said discharging mechanism and said drive mechanism such that said raw sealant resin is attached to said first surface except a tip portion of said protruded-shaped electrode.

3. (Original) The apparatus for manufacturing a semiconductor device according to claim 1, wherein said discharging mechanism is provided with a plurality of discharging nozzles.

4. (Original) The apparatus for manufacturing a semiconductor device according to claim 1, wherein said substrate holding unit is provided with a substrate temperature control mechanism for controlling a temperature of at least said semiconductor wafer substrate.

5. (Original) The apparatus for manufacturing a semiconductor device according to claim 1, further comprising at least two kinds of discharging mechanisms, each being capable of discharging respective different amounts of raw sealant resin.

6. (Original) The apparatus for manufacturing a semiconductor device according to claim 1, further comprising a heater for heating said raw sealant resin contained in said resin container unit.

7. (Original) The apparatus for manufacturing a semiconductor device according to claim 1, wherein said control unit controls said discharging mechanism and said drive mechanism such that said raw sealant resin is not attached to at least a portion of dicing lines of said semiconductor wafer substrate.

8. (Original) The apparatus for manufacturing a semiconductor device according to claim 1, wherein said control unit is adapted to control said discharging mechanism and said drive mechanism such that said raw sealant resin is not attached to dicing lines of said semiconductor wafer substrate and forms a layer with edges of a rounded shape in a vicinity of intersecting points of said dicing lines.

9. (Original) The apparatus for manufacturing a semiconductor device according to claim 5, wherein said control unit controls said discharging mechanism and said drive mechanism such that a first discharging mechanism of said at least two kinds of discharging mechanisms is capable of discharging droplets of raw sealant resin of an amount smaller than other discharging mechanisms used for discharging said raw sealant resin for an area in a vicinity of said electrode.

10. (Original) The apparatus for manufacturing a semiconductor device according to claim 6, wherein said control unit controls said discharging mechanism and said drive mechanism such that said raw sealant resin is not attached to at least a portion of dicing lines of said semiconductor wafer substrate.

11. (Original) The apparatus for manufacturing a semiconductor device according to claim 6, wherein said control unit controls said discharging mechanism and said drive mechanism such that said raw sealant resin is not attached to dicing lines of said semiconductor wafer substrate and forms a layer with edges of a rounded shape in vicinity of intersecting points of said dicing lines.

12-22 (Canceled)

23. (Previously Presented) An apparatus for manufacturing a semiconductor device, comprising:

substrate holding means for holding a semiconductor wafer substrate, wherein said substrate is provided with at least one electrode formed on a first surface thereof;

means for discharging droplets of raw sealant resin contained in a resin container unit through at least one discharging nozzle onto said first surface of said semiconductor wafer substrate held on said substrate holding unit;

drive means for displacing at least one of said semiconductor wafer substrate and said discharging nozzle;

means for controlling a discharging mechanism and a drive mechanism such that said raw sealant resin is attached to said first surface of said semiconductor wafer substrate excluding at least a portion of said electrode;

means for capturing image information of said semiconductor wafer substrate prior to droplets of raw sealant resin being discharged by said discharging means;

means for providing image information of said semiconductor wafer substrate; and

means for calculating a position, based upon said image information, for said discharging mechanism to discharge said droplets of raw sealant resin on said first surface of said semiconductor wafer substrate excluding at least a portion of said electrode, and for said drive mechanism to displace at least one of said semiconductor wafer substrate and said discharging nozzle.

24. (Original) The apparatus for manufacturing a semiconductor device according to claim 23, wherein said means for controlling controls said means for discharging and said drive means such that said raw sealant resin is attached to said first surface with the exception of a tip portion of said protruded-shaped electrode.

25. (Original) The apparatus for manufacturing a semiconductor device according to claim 23, wherein said means for discharging is provided with a plurality of discharging nozzle means.

26. (Original) The apparatus for manufacturing a semiconductor device according to claim 23, wherein said substrate holding means is provided with a substrate temperature control means for controlling temperature of at least said semiconductor wafer substrate.

27. (Original) The apparatus for manufacturing a semiconductor device according to claim 23, further comprising:

at least two kinds of means for discharging, each said discharging means being capable of discharging raw sealant resin in an amount different from the other.

28. (Original) The apparatus for manufacturing a semiconductor device according to claim 23, further comprising:

means for heating said raw sealant resin contained in said resin container means.

29. (Original) The apparatus for manufacturing a semiconductor device according to claim 23, wherein said means for controlling controls said means for discharging and said drive means such that said raw sealant resin is not attached to at least a portion of dicing lines of said semiconductor wafer substrate.

30. (Original) The apparatus for manufacturing a semiconductor device according to claim 23, wherein said means for controlling controls said means for discharging and said drive means such that said raw sealant resin is not attached to dicing lines of said semiconductor wafer substrate and forms a layer with edges of a rounded shape in vicinity of intersecting points of said dicing lines.

31. (Previously presented) The apparatus for manufacturing a semiconductor device according to claim 23, wherein said means for controlling controls said means for discharging and said drive means such that a first means for discharging, of at least two kinds of means for discharging, is capable of discharging droplets of raw sealant resin of an amount smaller than other means for discharging and said first means for discharging is used for discharging said raw sealant resin for an area in vicinity of said electrode.

32. (Original) The apparatus for manufacturing a semiconductor device according to claim 28, wherein said means for controlling controls said means for discharging and said drive means such that said raw sealant resin is not attached to at least a portion of dicing lines.

33. (Original) The apparatus for manufacturing a semiconductor device according to claim 28, wherein said means for controlling controls said means for discharging and said drive means such that said raw sealant resin is not attached to said dicing lines and forms a layer with edges of a rounded shape in vicinity of intersecting points of said dicing lines.

34. (Previously Presented) A semiconductor device manufacturing apparatus, comprising:

a semiconductor wafer substrate, said semiconductor wafer substrate having at least one electrode on a first surface thereof, and wherein said semiconductor wafer substrate is held in a substrate holding unit;

at least one discharging head for discharging droplets of raw sealant resin on said semiconductor wafer substrate and having at least one discharging nozzle;

a resin container unit connected to said discharging head and containing raw sealant resin;

a drive mechanism for displacing at least one of said semiconductor wafer substrate and said discharging head;

an image information camera for capturing image information of said semiconductor wafer substrate prior to said raw sealant resin being discharged by said discharging head; said image information device configured to provide said image information of said semiconductor wafer substrate; and

a control unit for controlling said discharging head and said drive mechanism,

wherein said control unit is adapted to calculate a position, based on said image information, for said discharging head to discharge droplets of raw sealant resin on said semiconductor wafer substrate excluding said at least one electrode, and for said drive mechanism to displace said at least one of said semiconductor wafer substrate.

35. (Original) The apparatus according to claim 34 wherein said at least one electrode has a protruded-shape.

36. (Original) The apparatus according to claim 35 wherein said control unit controls said discharging head and said drive mechanism such that said first surface of the semiconductor wafer substrate is covered by said raw sealant resin except for a tip portion of said protruded-shaped electrode.

37. (Original) The apparatus according to claim 34 wherein said discharging head comprises a plurality of discharging nozzles.

38. (Original) The apparatus according to claim 34 further comprising a temperature control mechanism for controlling a temperature of at least said semiconductor wafer substrate.

39. (Previously presented) The apparatus according to claim 34 wherein said discharging head further comprises at least two kinds of discharging mechanisms, each being capable of discharging respective different amounts of raw sealant resin.

40. (Original) The apparatus according to claim 34 wherein said resin container unit further comprises a heater for heating said raw sealant resin contained in said resin container unit.

APPENDIX B – EVIDENCE APPENDIX

NONE

APPENDIX C – RELATED PROCEEDINGS APPENDIX

NONE